MEMORY DEVICE COMPOSED OF A PLURALITY OF MEMORY CHIPS IN A SINGLE PACKAGE

Field of the Invention

[0001] This invention relates in general to memory devices, and, more particularly, to a memory device of a relatively large size comprising a plurality of memory chips each of a certain size, assembled in a single package with an array of input/output pins shared by the different memory chips, which may be singularly enabled by respective external commands.

Background of the Invention

[0002] To realize a high density memory device, for example of 128 Mbit, a possible approach includes assembling a plurality of memories (chips) of a certain size inside a single package, for example two memory chips of 64Mbit each. The so obtained memory has a storage size equal to the sum of the sizes of the single memory chips. The advantage of this approach is that it is not necessary to re-design a new integrated device.

[0003] This approach is largely used by manufacturers of memory devices. For sake of simplicity, the assembling of a twin stacked memory is described. The so-

called "twin stacked" memory is realized by assembling two memory chips or memories, generally identical, in a single package, bonding together the connection lines to the input/output pins of each memory in common on the array of input/output pins of the mounting frame of the package. According to known practice, the external enabling commands (commonly called chip enable or CE_N) are applied through distinct pins for commanding separately the two memories.

[0004] Figure 1 depicts a classic structure of a "twin stacked" device. The bus of external addresses APD and DQPAD and the control signals OE_N, WE_N, RP_N are connected in common for constituting the equivalent array of input/output pins of the device. By contrast, the CE_N pins are multiple, that is each one is dedicated to a respective memory, and depending on the configuration of logic signals applied to them, four different combinations are possible, that may be selected by the user through dedicated external commands. The user may select one or the other of the two memories by lowering the respective logic "chip enable" command (CE), or place both memories in stand-by by forcing both "chip enable" commands to a high logic level.

[0005] There is a risk of both commands accidentally switching low, thus activating in parallel both memories. In any case, the system must manage a plurality of "chip enable" commands specific for the distinct memory chips contained in the packaged device.

Summary of the Invention

[0006] An object of the present invention is to provide a method of managing a plurality of enable

commands to respective memory chips for selecting the memory to which a certain read, delete or write command pertains, that is more effective and reliable.

[0007] The invention includes the use of a single external chip enable command that is applied through a single pin of the multi-chip device, thus rendering the stacked memory device perfectly similar, from the user's point of view, to a normal "stand alone" memory of capacity equal to the sum of capacities of the distinct memory chips that are included in the packaged device.

[0008] This ideal situation that practically eliminates the risk of accidentally activating more than one memory chip at the time is made possible by realizing, on each memory chip, $2*n$ additional input/output pads, wherein n is such that 2^n is the number of distinct memory chips that compose the stacked memory device, and a circuit for generating internally an enable/disable command of the memory chip. This circuit comprises $2*n$ buffers, each coupled to a respective additional pad, and a combinatory logic circuit, input with the output signals of the buffers corresponding to the logic state of the additional pads and with the single external enable signal, that generates the internal enable/disable command of the memory chip.

[0009] In practice, one or a plurality (n) of the additional I/O pads of each memory chip are hardwired to a certain logic state for example either grounded (GND) or connected to the supply rail (VDD), in different combinations for the distinct memory chips, to distinguish the different memory chips, while the other additional pad or (n) pads are connected to the

input/output pin or pins corresponding to the most significant bit or bits of the bus of external addresses.

[0010] The combinatory logic generates an enable/disable signal of the coded memory as a function of the biasing of the additional hardwired pad or pads, of the most significant bit or bits of the external address and of the logic value of the single external enable command:

- by switching high the external enable signal, all memory chips will be configured in stand-by;
- by switching low the external enable signal, only one memory chip among all the memory chips assembled in the same device will be enabled, depending on the logic configuration of these additional pads.

[0011] In practice, the user sees only a "stand alone" memory device of a capacity corresponding to the sum of the storage capacities of the memories composing it, and has to manage only a single enable/disable command.

Brief Description of the Drawings

[0012] FIG. 1 is a schematic diagram of a conventional twin stacked device.

[0013] FIG. 2 is a schematic diagram illustrating each memory chip and the additional circuits according to the present invention.

[0014] FIG. 3 is a schematic diagram illustrating a twin stacked device according to the present invention.

[0015] FIG. 4 is a schematic diagram illustrating a stacked device including four distinct memories mounted in a same package according to another embodiment of the present invention.

Detailed Description of the Preferred Embodiments

[0016] Referring to Figure 2, according to this invention, in each of the two memory chips DEV#1 and DEV#2 to be mounted inside a single package for realizing a memory device of doubled storage capacity, two additional pads are realized, APAD<MSB> and DEV_PAD, structurally equivalent to the other input/output pads that are usually present. Respective input buffers IN_BUFFER are functionally coupled to the two additional pads and a combinatory logic circuit R.C. is input with the outputs AIN<MSB> and DEV of the two input buffers and with the external enable command CE_N and outputs an internally generated command CEN_INT for enabling/disabling the memory chip.

[0017] Figure 3 depicts a twin stacked device realized according this invention. The additional pad DEV_PAD of the first memory DEV#1 is grounded while the second pad DEV_PAD of the second memory DEV#2 is connected to the supply voltage node, thus logically distinguishing the two memory chips. The most significant bit of the external address bus (that is added in doubling the capacity of the device, for instance from 64Mbit to 128Mbit) is used for selecting one or the other of the two memory chips, rendered logically distinguishable by the different biasing of their additional pad DEV_PAD.

[0018] To this end, the additional pads APAD<MSB> of the two memory chips DEV#1 and DEV#2 are connected in common to the corresponding external pin APAD<MSB> of the device. This connection is represented by the two arrows oriented towards the input/output pin corresponding to the most significant bit APAD<MSB> of the external

address bus of the device (for sake of simplicity isolatedly shown in Figure 2).

[0019] The pads CE_N of the two memories DEV#1 and DEV#2 dedicated to receive the enable/disable command, are connected in common to the unique input pin (CE_N) of the composite memory device dedicated to receive the external enable/disable command. The logic combinatory logic circuit R.C., realized in each of the two memory chips DEV#1 and DEV#2, generates the internal enable/disable command CEN_INT according to the following exemplary truth table of the logic states of the two additional pads DEV_PAD and APAD<MSB> and of the external unique command CE_N.

	CEN_N	DEV_PAD	APAD<MSB>	CEN_INT
DEV#1	0	0	0	0 (active)
	0	0	1	1 (standby)
DEV#2	0	1	0	1 (standby)
	0	1	1	0 (active)
	1	-	-	1 (standby)

[0020] It may be noted that by switching high the logic value of the unique external command CE_N, a stand-by condition of both memory chips is implemented and thus of the composite device as a whole. By switching low the external command CE_N, the device appears to the user as behaving as a "stand alone" memory of capacity equivalent to the sum of the capacities of the two memories contained therein. In fact, depending on the logic value of APAD<MSB> only one of the two memories is enabled.

[0021] This approach may be extended also to devices containing even a larger number of memory chips. The case of a memory device realized by mounting inside a single

package four memory chips DEV#1, DEV#2, DEV#3 and DEV#4 is schematically depicted in Figure 4, for instance for constituting a 256 Mbit memory using four memory chips of 64Mbit each.

[0022] In this case each memory chip will be provided with a total of four additional pads in view of the fact that the input/output address bus of the multi-chip device must be incremented of two additional bits (this is dictated by passing from a 64Mbit memory to a 256Mbit memory) and in this case two most significant bits <MSB> and <MSB-1> of the external addresses must be used for selecting the memory to which the external address pertains to. The four pairs of additional pads DEV_PAD<1,0> of the four distinct memory chips are logically configured differently from one another, by grounding or connecting both to the supply voltage node or one to the supply voltage node and the other to the ground node or vice versa, according to a scheme of connections such as the one shown in Figure 4.

[0023] In this case, besides the external enable/disable command CE_N, the combinatory logic circuit will receive the logic values corresponding to the hardwired configuration of the two additional pads DEV_PAD<1,0> of each memory and the two most significant bits of the external address that are applied respectively to the corresponding additional input/output pads APAD<MSB,MSB-1> of all four memories, for generating an internal enable/disable command CEN_INT according to the following exemplary truth table.

	CEN_N	DEV_PAD<1,0>		APAD<MSB,MSB-1>		CEN_INT
DEV#1	0	0	0	0	0	0 (active)
	0	0	0	0	1	1 (standby)
	0	0	0	1	0	1 (standby)
	0	0	0	1	1	1 (standby)
DEV#2	0	0	1	0	0	1 (standby)
	0	0	1	0	1	0 (active)
	0	0	1	1	0	1 (standby)
	0	0	1	1	1	1 (standby)
DEV#3	0	1	0	0	0	1 (standby)
	0	1	0	0	1	1 (standby)
	0	1	0	1	0	0 (active)
	0	1	0	1	1	1 (standby)
DEV#4	0	1	1	0	0	1 (standby)
	0	1	1	0	1	1 (standby)
	0	1	1	1	0	1 (standby)
	0	1	1	1	1	0 (active)
	1	-	-	-	-	1 (standby)

[0024] Even in this embodiment the composite device will appear to the user like a "stand alone" memory of equivalent capacity. The unique external "chip enable" command CE_N will enable or disable the whole memory device while the first two bit of the address string are exploited for operating a selection among the four memories contained in the device, of the memory to which the addressed memory location pertains, in a way that is not perceived by the user and that is reliably performed by virtue of the fixed biasing of the DEV_PAD nodes (hardwired) by the combinatory logic circuit that is purposely realized on each of the four memory chips that compose the device. The stated objectives and advantages are attained by the architecture of this invention.